REMARKS

I. Summary of Office Action

In the Office Action mailed December 7, 2005, Examiner objected to claims 3, 6 19, 21, 25, 36, and 40 for various informalities. Under 35 U.S.C. § 102(e), Examiner rejected claims 1-8, 19-20, 23, 32-33, 40-41, 44-45, and 56-60 as being anticipated by published U.S. Patent Application Publication No. 2002/0175713 A1 (Knowles), and claims 1-8, 19-20, 23, 25-27, 32-33, 40-41, 44-45, and 56-60 as being anticipated by U.S. Patent Application Publication No. 6,327,176 (Li). In addition, under 35 U.S.C. § 103(a), Examiner rejected claims 16-18 as being unpatentable over the combination of Knowles and Li.

On the other hand, Examiner allowed claims 48-55, and also claims 9-15, 21-22, 24, 28-31, 34-39, 42-43, and 46-47 so long as they are rewritten into independent form. Applicant thanks Examiner for indicating the allowable subject matter.

II. Status of the Claims

Applicant has amended claims 3, 6, 19, 21, 25, 36 and 40 to correct for informalities. Applicant has also canceled claims 2, 5, 35, 39, 43, and 56, and amended claim 1 to further clarify the claimed subject matter. In addition, Applicant has amended claims 3, 4, 6, and 7 to depend from claim 1.

Now pending in this application are claims 1, 3-4, 6-34, 36-38, 40-42, 44-55, and 57-60, of which claims 1, 48, and 57-60 are independent, and the rest are dependent.

The invention as claimed in each of claims 1, 3-4, 6-34, 36-38, 40-42, and 44-55 includes a system for hardening a logic circuit against at least one of a single-event upset and single-event transient condition, the system comprising in combination (i) a logic circuit outputting independently-obtained first and second redundant signals; (ii) first and second feed-forward

devices, wherein each of the first and second feed-forward devices is operable to receive both of the first and second redundant signals, and wherein when the first and second redundant signals are in expected states, then (a) the first feed-forward device responsively provides a first feed-forward signal and (b) the second feed-forward device responsively provides a second feed-forward signal, and wherein when the first and second redundant signals are in unexpected states, then both the first and second feed-forward devices continue to provide their respective feed-forward signals consistent with the last expected state of the redundant signals; and (iii) first and second feedback devices, wherein each of the first and second feedback devices is operable to receive both of the first and second feed-forward signals, and wherein when the first and second feed-forward signals are in expected states, (a) the first feedback device responsively feeds a first feedback signal back to the first redundant signal and (b) the second feedback device responsively feeds a second feedback signal back to the second redundant signal, and wherein when at least one of the first and second feed-forward signals is in an unexpected state, then both the first and second feedback devices continue to provide their respective feedback signals consistent with the last expected state of the feed-forward signals.

The invention as claimed in claims 57-60 includes similar functions, but is focused on either the first redundant signal, the second redundant signal, the input signal to the first feedback device, or the input signal to the second feedback device being in an unexpected state. In any of these scenarios, the first and second feed-forward devices and the first and second feedback devices are all still "operable to not change [the] current state of" their respective signals.

III. Response to Rejections

a. Response to 35 U.S.C. § 102(e) Rejection of Independent Claim 1

The Examiner rejected claim 1 under 35 U.S.C. § 102(e) as being anticipated by both Knowles and Li. For a reference to anticipate a claim, the cited reference must teach each and every element of the claim. MPEP § 2131. Applicants respectfully traverse the rejection of claim 1 because as amended, both Knowles and Li fail to teach each and every element of claim 1. Namely, both Knowles and Li fail to teach "when the first and second redundant signals are in unexpected states, then both the first and second feed-forward devices continue to provide their respective feed-forward signals consistent with the last expected state of the redundant signals."

Both Knowles and Li disclose logic architecture that is hardened to single event upset conditions. See Knowles Abstract; Li Abstract. Similarly, both Knowles and Li disclose the use of dual port inverter pairs in the said logic architecture. See Knowles, Figs. 1 and 3; Li, Fig. 4, label 44. However, by virtue of Knowles' and Li's use of dual port inverter pairs in their logic architecture, when an input value to any one of the dual port inverter pairs is in unexpected state, the output value to at least one dual port inverter of the pair will be in a state of contention. See Knowles Fig. 8; ¶ 0040. In this state, the output value of a given dual port inverter will depend upon the relative strength of each transistor comprising the dual port inverter, and therefore, may switch from the last expected state. Thus, at least one dual port inverter of a pair may fail to provide a signal "consistent with the last expected state."

In Knowles, for example, when the input values to the two dual port inverters are both equal to 0, i.e. in an expected state, then their respective output values are both 1. See Knowles Figs. 3 and 8; ¶ 0035. However, when one of the input values temporarily shifts to a logic value of 1 due to a single event upset condition, and is in an unexpected state, rather than both dual

port inverters providing an output "consistent with the last expected state," at least one dual port inverter will provide an output whose value is "undefined." See Knowles Fig. 8; ¶ 0040. (when the input values to the PMOS and NMOS are 0, and a transient pulse drives the input to the NMOS to 1, then both the PMOS and NMOS transistors "are both in an on state. Thus, second inverter's PMOS and NMOS transistors . . . are temporarily in a state of contention, and the value of [the] output signal . . . depends upon the relative strength of each transistor. . . . Thus when [the inputs] . . . equal 0, and while [the transient pulse] equals 1, the state of [the output] signal is undefined.").

Similarly, the dual port inverter pair 44 in Fig. 4 of Li operates in a likewise manner. When the two input values to dual port inverter pair 44 are 0 (or 1), i.e. in an expected state, then their respective output values are both 1 (or 0). However, when the input values to the dual port inverter pair are at different logic levels due to a single event upset condition, and are therefore in an unexpected state, rather than both dual port inverters maintaining an output "consistent with the last expected state," the output value to at least one of the dual port inverters is "invalid." See Li, Fig. 4; col. 4, lines 32-39 ("when inputs IN1 and IN2 are different, both outputs OUT1 and OUT2 are invalid. Thus, data at both inputs IN1 and IN2 must be the same in order to generate a valid output at either OUT1 and OUT2.").

Hence, in both Knowles and Li, when an input value to the dual port inverter pair experiences a logic shift due to a single event upset condition, at least one of the dual port inverters will be in a state of contention. In this state, the output value of a given dual port inverter will depend upon the relative strength of each transistor comprising the dual port inverter, and therefore, may switch from the last expected state. Thus, at least one dual port inverter of a pair may fail to provide a signal "consistent with the last expected state." As such,

both Knowles and Li fail to teach "when the first and second redundant signals are in unexpected states, then both the first and second feed-forward devices continue to provide their respective feed-forward signals consistent with the last expected state of the redundant signals."

As such, both Knowles and Li fail to teach each and every element of claim 1. Thus, Applicants respectfully submit that claim 1 is in condition for allowance.

b. Response to 35 U.S.C. § 102(e) Rejections of Independent Claims 57-60

The Examiner also rejected claims 57-60 under 35 U.S.C. § 102(e) as being anticipated by both Knowles and Li. As noted, for a reference to anticipate a claim, the cited reference must teach each and every element of the claim. MPEP § 2131. Applicants respectfully traverse the rejection of claims 57-60 because both Knowles and Li fail to teach each and every element of claims 57-60. Namely, both Knowles and Li fail to teach when either the first redundant signal, the second redundant signal, the input signal to the first feedback device, or the input signal to the second feedback device are in an unexpected state, then the first and second feed-forward devices and the first and second feedback devices are all still "operable to not change [the] current state of" their respective signals.

As disclosed in the figures, both Knowles and Li teach the use of two dual port inverter pairs in their single event upset hardened logic architecture. See Knowles, Figs. 1 and 3; Li, Fig. 4. For the reasons set forth above, by virtue of Knowles' and Li's use of dual port inverter pairs in their logic architecture, when an input value to either pair of dual port inverters is in an unexpected state, the transistors of the given dual port inverter are temporarily in a state of contention, and the value of the output signal of the dual port inverter will depend upon the relative strength of each transistor. See Knowles Fig. 8; ¶ 0040. Because the output value of a given dual port inverter pair will depend upon the relative strength of each transistor in this

condition, the output value may switch from the last expected state. Therefore, at least one dual port inverter of the dual port inverter pair may fail to provide a signal "consistent with the last expected state."

Therefore, both Knowles and Li fail to teach when either the first redundant signal, the second redundant signal, the input signal to the first feedback device, or the input signal to the second feedback device are in an unexpected state, then the first and second forward-feed devices and the first and second feedback devices are all still "operable to not change [the] current state of" their respective signals. As such, both Knowles and Li fail to teach each and every element of claims 57-60. Thus, Applicants respectfully submit that claims 57-60 are in condition for allowance.

c. Dependent Claims

Without addressing the merits of Examiner's statements regarding the pending dependent claims 3-4, 6-34, 36-38, 40-42, 44-47, and 49-55, which are not conceded, Applicant points out that these claims depend from and include all of the limitations of independent claim 1. Therefore, Applicant's dependent claims distinguish the cited references for the same reasons discussed above with regard to independent claim 1. Applicant respectfully requests that Examiner withdraw the rejections of the pending dependent claims.

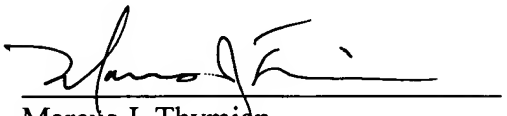
CONCLUSION

For the foregoing reasons, Applicant submits that all of the pending claims are now in condition for allowance. Applicant thus respectfully requests favorable reconsideration and allowance. Examiner is invited to contact the undersigned attorney at 312-935-2352, should any questions arise.

Respectfully submitted,

McDONNELL BOEHNEN HULBERT & BERGHOFF LLP

Date: March 7, 2005

By: 

Marcus J. Thymian
Reg. No. 43,954